AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

Claims 1-10 (Cancelled)

Claim 11 (Currently Amended): ~~The~~ A method for manufacturing ~~the~~ a semiconductor device ~~according to claim 10, wherein~~ for forming a wiring by a dual damascene method, the method comprising the steps of:

forming a mask for a wiring trench patterned to be a wiring trenches pattern on an interlayer dielectric film;

forming a mask for a via hole patterned to be a via holes pattern on the mask for the wiring trench by using a multilayered resist;

forming a hole shallower than a thickness of the interlayer dielectric film in the interlayer dielectric film by processing the interlayer dielectric film, using the mask for the via hole;

forming a wiring trench in the interlayer dielectric film by processing the interlayer dielectric film, using the mask for the wiring trench, and simultaneously forming a via hole by passing the hole through a base layer; and

embedding a wiring material in the wiring trench and said via hole, wherein

said step of forming the mask for the via hole includes the steps of:

forming an organic film, an inorganic film, and a photoresist layer in this order on the mask for the wiring trench;

processing the photoresist layer so as to be a plane shape to the via hole;

processing the inorganic film so as to be a plane shape to the via hole by using the photoresist layer as a mask; and

processing the organic film so as to be a plane shape to the via hole by using the inorganic film as a mask, and simultaneously removing the photoresist layer, and

said step of forming the hole includes a step of processing the mask for the wiring trench so as to be a plane shape to the via hole by using the organic film as a mask, and simultaneously removing the inorganic film, and

the organic film is removed while forming the hole.

Claims 12-13 (Cancelled)

Claim 14 (Currently Amended): ~~The~~ A method for manufacturing ~~the~~ a semiconductor device ~~according to claim 13, wherein~~ for forming a wiring by a dual damascene method, the method comprising the steps of:

forming a mask for a wiring trench patterned to be a wiring trenches pattern on an interlayer dielectric film;

forming a mask for a via hole patterned to be a via holes pattern on the mask for the wiring trench by using a multilayered resist;

forming a hole shallower than a thickness of the interlayer dielectric film in the interlayer dielectric film by processing the interlayer dielectric film, using the mask for the via hole;

forming a wiring trench in the interlayer dielectric film by processing the interlayer dielectric film, using the mask for the wiring trench, and simultaneously forming a via hole by passing the hole through a base layer; and

embedding a wiring material in the wiring trench and said via hole, wherein

said step of forming the mask for the via hole includes the steps of:

forming an organic film and a photoresist layer containing Si in this order on the mask for the wiring trench,

processing the photoresist layer so as to be a plane shape to the via hole; and

processing the organic film so as to be a plane shape to the via hole by using the photoresist layer as a mask, and

said step of forming the hole includes a step of processing the mask for the wiring trench so as to be a plane shape to the via hole by using the organic film as a mask, and simultaneously removing the photoresist, and

the organic film is removed while forming the hole.

Claims 15-18 (Cancelled)

Claim 19 (New): The method for manufacturing the semiconductor device according to claim 11, wherein

said step of forming the mask for the wiring trench includes the steps of:

forming a first, a second, and a third hard mask in this order on the interlayer dielectric film; and

processing the third hard mask so as to be a plane shape to the wiring trench, and

wherein the second hard mask is made from a different material from the first and the third hard mask.

Claim 20 (New): The method for manufacturing the semiconductor device according to claim 19, wherein

each of the first to the third hard mask is made from one kind of inorganic material selected from the group consisting of silicon nitride, silicon dioxide, silicon carbide, amorphous hydrogenated silicon carbide, silicon carbide nitride, organo-silicate glass, silicon rich oxide, tetraethylorthosilicate glass, phosphosilicate glass, organic siloxane polymer, carbon doped silicate glass, hydrogen doped silicate glass, silsesquioxane glass, spin-on glass, and fluorinated silicate glass.

Claim 21 (New): The method for manufacturing the semiconductor device according to claim 19, wherein

the first hard mask is between 30 nm and 100 nm thick;

the second hard mask is between 50 nm and 200 nm thick; and

the third hard mask is between 30 nm and 100 nm thick.

Claim 22 (New): The method for manufacturing the semiconductor device according to claim 11, wherein

the interlayer dielectric film is made from an organic material.

Claim 23 (New): The method for manufacturing the semiconductor device according to claim 11, wherein

a spin-on glass film is formed as the inorganic film.

Claim 24 (New): The method for manufacturing the semiconductor device according to claim 11, wherein

a thickness of the inorganic film is thinner than a thickness of the mask for the wiring trench.

Claim 25 (New): The method for manufacturing the semiconductor device according to claim 11, wherein

the organic film is between 100 nm and 400 nm thick;

the inorganic film is between 30 nm and 200 nm thick; and

the photoresist layer is between 100 nm and 300 nm thick, supposing the interlayer dielectric film is between 100 nm and 600 nm thick.

Claim 26. (New): The method for manufacturing the semiconductor device according to claim 11, wherein

a thickness of the organic film is thinner than that of the interlayer dielectric film.

Claim 27 (New): The method for manufacturing the semiconductor device according to claim 11, wherein

a film exposed by light at a wavelength of 248 nm, 193 nm, or 157 nm is formed as the photoresist layer.

Claim 28 (New): The method for manufacturing the semiconductor device according to claim 14, wherein

said step of forming the mask for the wiring trench includes the steps of:

forming a first, a second, and a third hard mask in this order on the interlayer dielectric film; and

processing the third hard mask so as to be a plane shape to the wiring trench, and

wherein the second hard mask is made from a different material from the first and the third hard mask.

Claim 29 (New) The method for manufacturing the semiconductor device according to claim 28, wherein

each of the first to the third hard mask is made from one kind of inorganic material selected from the group consisting of silicon nitride, silicon dioxide, silicon carbide, amorphous hydrogenated silicon carbide, silicon carbide nitride, organo-silicate glass, silicon rich oxide, tetraethylorthosilicate glass, phosphosilicate glass, organic siloxane polymer, carbon doped silicate glass, hydrogen doped silicate glass, silsesquioxane glass, spin-on glass, and fluorinated silicate glass.

Claim 30 (New) The method for manufacturing the semiconductor device according to claim 28, wherein

the first hard mask is between 30 nm and 100 nm thick;

the second hard mask is between 50 nm and 200 nm thick; and

the third hard mask is between 30 nm and 100 nm thick.

Claim 31 (New) The method for manufacturing the semiconductor device according to claim 14, wherein

The interlayer dielectric film is made from an organic material.

Claim 32. (New): The method for manufacturing the semiconductor device according to claim 14, wherein

a thickness of the organic film is thinner than that of the interlayer dielectric film.

Claim 33. (New): The method for manufacturing the semiconductor device according to claim 14, wherein

A film exposed by light at a wavelength of 248 nm, 193 nm, or 157 nm, is formed as the photoresist layer.